Opcode Chart

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Op7 | | | Ra5 | | Rt5 | | | Imm25 | | | | | | | | | | |  |  | |
| 0 | | |  | |  | | |  | | | | | | | | | | | Misc | Miscellaneous | |
| 0 | | | ---28 | | | | | | | | | | | | 0 | | | | BRK |  | |
| 0 | | |  | | | | | | | | | | | | 2 | | | | IRET | Return from interrupt | |
| 0 | | |  | | | | | | | | | | | | 3 | | | | ERET | Return from exception | |
| 0 | | |  | | | | | | | | | | | | 40 | | | | WAIT |  | |
| 0 | | |  | | | | | | | | | | | | 49 | | | | TLBP | Probe TLB entries | |
| 0 | | |  | | | | | | | | | | | | 50 | | | | TLBR | Read TLB entry | |
| 0 | | |  | | | | | | | | | | | | 51 | | | | TLBWI | Write TLB entry using index | |
| 0 | | |  | | | | | | | | | | | | 52 | | | | TLBWR | Write random TLB entry | |
| 0 | | |  | | | | | | | | | | | | 64 | | | | CLI | Clear interrupt mask | |
| 0 | | |  | | | | | | | | | | | | 65 | | | | SEI | Set interrupt mask | |
| 0 | | |  | |  | |  | | | | | | | | | | | |  |  | |
| 1 | | | Ra5 | | Rt5 | | Rc5 | | Op13 | | | | | | Opcd7 | | | | {reg} | register operate | |
| 1 | | | Ra5 | | Rt5 | |  | |  | | | | | | 4 | | | | COM | compliment | |
| 1 | | | Ra5 | | Rt5 | |  | |  | | | | | | 5 | | | | NOT | Logical not | |
| 1 | | | Ra5 | | Rt5 | |  | |  | | | | | | 6 | | | | NEG | Negative -a | |
| 1 | | | Ra5 | | Rt5 | |  | |  | | | | | | 7 | | | | ABS | Absolute value (a) | |
| 1 | | | Ra5 | | Rt5 | |  | |  | | | | | | 9 | | | | MOV | Rt = a | |
| 1 | | | Ra5 | | Rt5 | |  | |  | | | | | | 13 | | | | SWAP | Swap register halves | |
| 1 | | | Ra5 | | Rt5 | |  | |  | | | | | | 16 | | | | CTLZ | Count leading zeros | |
| 1 | | | Ra5 | | Rt5 | |  | |  | | | | | | 17 | | | | CTLO | Count leading ones | |
| 1 | | | Ra5 | | Rt5 | |  | |  | | | | | | 18 | | | | CTPOP | Count population | |
| 1 | | | Ra5 | | Rt5 | |  | |  | | | | | | 19 | | | | SEXT8 | Sign extend 8 to 64 bits | |
| 1 | | | Ra5 | | Rt5 | |  | |  | | | | | | 20 | | | | SEXT16 | Sign extend 16 to 64 bits | |
| 1 | | | Ra5 | | Rt5 | |  | |  | | | | | | 21 | | | | SEXT32 | Sign extend 32 to 64 bits | |
| 1 | | | Ra5 | | Rt5 | |  | |  | | | | | | 24 | | | | SQRT | Square root | |
| 1 | | |  | | Rt5 | |  | |  | | SPR6 | | | | 40 | | | | MFSPR | Move from special register | |
| 1 | | | Ra5 | |  | |  | |  | | SPR6 | | | | 41 | | | | MTSPR | Move to special register | |
| 1 | | | Ra5 | | Rt5 | |  | |  | | | | | | 50 | | | | OMG | Open mutex gate | |
| 1 | | | Ra5 | |  | |  | |  | | | | | | 51 | | | | CMG | Close mutex gate | |
| 1 | | |  | | Rt5 | |  | |  | | Gate6 | | | | 52 | | | | OMGI | Open mutex gate | |
| 1 | | |  | |  | |  | |  | | Gate6 | | | | 53 | | | | CMGI | Close mutex gate | |
| 1 | | |  | | Rb5 | |  | |  | | | | | | 58 | | | | EXEC | Execute instruction | 3 |
| 1 | | | Ra5 | | Rb5 | | Rc5 | | Rt5 | | |  | | | 59 | | | | MYST | Mystery operation | 1 |
| 2 | | | Ra5 | | Rb5 | | Rt5 | | Op10 | | | | |  | 27 | | | | ADD | a + b, error on overflow | |
| 2 | | | Ra5 | | Rb5 | | Rt5 | | Op10 | | | | |  | 37 | | | | ADDU | a + b, no errors | |
| 2 | | | Ra5 | | Rb5 | | Rt5 | | Op10 | | | | |  | 47 | | | | SUB | a - b, error on overflow | |
| 2 | | | Ra5 | | Rb5 | | Rt5 | | Op10 | | | | |  | 57 | | | | SUBU | a - b, no errors | |
| 2 | | | Ra5 | | Rb5 | | Rt5 | | Op10 | | | | |  | 67 | | | | CMP | compare | |
| 2 | | | Ra5 | | Rb5 | | Rt5 | | Op10 | | | | |  | 77 | | | | CMPU |  | |
| 2 | | | Ra5 | | Rb5 | | Rt5 | | Op10 | | | | |  | 87 | | | | AND |  | |
| 2 | | | Ra5 | | Rb5 | | Rt5 | | Op10 | | | | |  | 97 | | | | OR |  | |
| 2 | | | Ra5 | | Rb5 | | Rt5 | | Op10 | | | | |  | 107 | | | | XOR | Exclusive or | |
| 2 | | | Ra5 | | Rb5 | | Rt5 | | Op10 | | | | |  | 117 | | | | ANDC |  | |
| 2 | | | Ra5 | | Rb5 | | Rt5 | | Op10 | | | | |  | 127 | | | | NAND |  | |
| 2 | | | Ra5 | | Rb5 | | Rt5 | | Op10 | | | | |  | 137 | | | | NOR |  | |
| 2 | | | Ra5 | | Rb5 | | Rt5 | | Op10 | | | | |  | 147 | | | | XNOR |  | |
| 2 | | | Ra5 | | Rb5 | | Rt5 | | Op10 | | | | |  | 15 | | | | ORC | Or with complement | |
| 2 | | | Ra5 | | Rb5 | | Rt5 | | Op10 | | | | |  | 20 | | | | MIN | Minimum of a or b | |
| 2 | | | Ra5 | | Rb5 | | Rt5 | | Op10 | | | | |  | 21 | | | | MAX | Maximum of a or b | |
| 2 | | | Ra5 | | Rb5 | | Rt5 | | Op10 | | | | |  | 24 | | | | MULU | Unsigned multiply | |
| 2 | | | Ra5 | | Rb5 | | Rt5 | | Op10 | | | | |  | 25 | | | | MULS | Signed multiply | |
| 2 | | | Ra5 | | Rb5 | | Rt5 | | Op10 | | | | |  | 26 | | | | DIVU | Unsigned divide | |
| 2 | | | Ra5 | | Rb5 | | Rt5 | | Op10 | | | | |  | 27 | | | | DIVS | Signed divide | |
| 2 | | | Ra5 | | Rb5 | | Rt5 | | Op10 | | | | |  | 30 | | | | MOVZ | Conditional move if zero | |
| 2 | | | Ra5 | | Rb5 | | Rt5 | | Op10 | | | | |  | 31 | | | | MOVNZ | Conditional move if not zero | |
| 2 | | | Ra5 | | Rb5 | | Rt5 | | Op10 | | | | |  | 40 | | | | SHL | Shift left | |
| 2 | | | Ra5 | | Rb5 | | Rt5 | | Op10 | | | | |  | 41 | | | | SHRU | Unsigned Shift right | |
| 2 | | | Ra5 | | Rb5 | | Rt5 | | Op10 | | | | |  | 42 | | | | ROL | Rotate left | |
| 2 | | | Ra5 | | Rb5 | | Rt5 | | Op10 | | | | |  | 43 | | | | ROR | Rotate right | |
| 2 | | | Ra5 | | Rb5 | | Rt5 | | Op10 | | | | |  | 44 | | | | SHR | Signed shift right | |
| 2 | | | Ra5 | | Rb5 | | Rt5 | |  | Me6 | | | Mb6 | | 45 | | | | ROLAM | Rotate left and mask | |
|  | | |  | |  | |  | |  | | | | | |  | | | |  |  | |
|  | | |  | |  | |  | |  | | | | | |  | | | |  |  | |
| 2 | | | Ra5 | | Rb5 | | Rt5 | | Op10 | | | | |  | 96 | | | | SLT |  | |
| 2 | | | Ra5 | | Rb5 | | Rt5 | | Op10 | | | | |  | 97 | | | | SLE |  | |
| 2 | | | Ra5 | | Rb5 | | Rt5 | | Op10 | | | | |  | 98 | | | | SGT |  | |
| 2 | | | Ra5 | | Rb5 | | Rt5 | | Op10 | | | | |  | 99 | | | | SGE |  | |
| 2 | | | Ra5 | | Rb5 | | Rt5 | | Op10 | | | | |  | 100 | | | | SLTU |  | |
| 2 | | | Ra5 | | Rb5 | | Rt5 | | Op10 | | | | |  | 101 | | | | SLEU |  | |
| 2 | | | Ra5 | | Rb5 | | Rt5 | | Op10 | | | | |  | 102 | | | | SGTU |  | |
| 2 | | | Ra5 | | Rb5 | | Rt5 | | Op10 | | | | |  | 102 | | | | SGEU |  | |
| 2 | | | Ra5 | | Rb5 | | Rt5 | | Op10 | | | | |  | 104 | | | | SEQ |  | |
| 2 | | | Ra5 | | Rb5 | | Rt5 | | Op10 | | | | |  | 105 | | | | SNE |  | |
| 3 | | |  | |  | |  | |  | | | | | |  | | | |  |  | |
| 3 | | | Ra5 | | Rt5 | | Imm6 | | | Me6 | | | Mb6 | | Sz | | 0 | | SHLI | Shift left | |
| 3 | | | Ra5 | | Rt5 | | Imm6 | | | Me6 | | | Mb6 | | Sz | | 1 | | SHRUI | Unsigned shift right | |
| 3 | | | Ra5 | | Rt5 | | Imm6 | | | Me6 | | | Mb6 | | Sz | | 2 | | ROLI | Rotate left | |
| 3 | | | Ra5 | | Rt5 | | Imm6 | | | Me6 | | | Mb6 | | Sz | | 3 | | SHRI | Shift right | |
| 3 | | | Ra5 | | Rt5 | | Imm6 | | | Me6 | | | Mb6 | | Sz | | 4 | | RORI | Rotate right | |
| 3 | | | Ra5 | | Rt5 | | Imm6 | | | Me6 | | | Mb6 | | Sz | | 5 | | ROLAMI | Rotate left and mask | |
| 3 | | | Ra5 | | Rt5 | | Imm6 | | | Me6 | | | Mb6 | | Sz | | 8 | | BFINS | Bit field insert | |
| 3 | | | Ra5 | | Rt5 | | Imm6 | | | Me6 | | | Mb6 | | Sz | | 9 | | BFSET | Bit field set | |
| 3 | | | Ra5 | | Rt5 | | Imm6 | | | Me6 | | | Mb6 | | Sz | | 10 | | BFCLR | Bit field clear | |
| 3 | | | Ra5 | | Rt5 | | Imm6 | | | Me6 | | | Mb6 | | Sz | | 11 | | BFCHG | Bit field change | |
|  | | |  | |  | |  | |  | | | | | |  | | | |  |  | |
|  | | |  | |  | |  | |  | | | | | |  | | | |  |  | |
|  | | |  | |  | |  | |  | | | | | |  | | | |  |  | |
|  | | |  | |  | |  | |  | | | | | |  | | | |  |  | |
| Basic Arithmetic | | | | | | | | | | | | | | | | | | | | | |
| 4 | | | Ra5 | | Rt5 | | Imm25 | | | | | | | | | | | ADDI | | Add immediate | |
| 5 | | | Ra5 | | Rt5 | | Imm25 | | | | | | | | | | | ADDUI | | Add immediate | |
| 6 | | | Ra5 | | Rt5 | | Imm25 | | | | | | | | | | | SUBI | | Subtract immediate | |
| 8 | | | Ra5 | | Rt5 | | Imm25 | | | | | | | | | | | CMPI | | Compare immediate | |
| 9 | | | Ra5 | | Rt5 | | Imm25 | | | | | | | | | | | CMPUI | | Unsigned compare immediate | |
| 10 | | | Ra5 | | Rt5 | | Imm25 | | | | | | | | | | | ANDI | | And | |
| 11 | | | Ra5 | | Rt5 | | Imm25 | | | | | | | | | | | ORI | | Or | |
| 12 | | | Ra5 | | Rt5 | | Imm25 | | | | | | | | | | | XORI | | Exclusive or | |
| 13 | | | Ra5 | | Rt5 | | Imm25 | | | | | | | | | | | MULUI | | Unsigned multiply | |
| 14 | | | Ra5 | | Rt5 | | Imm25 | | | | | | | | | | | MULSI | | Signed multiply | |
| 15 | | | Ra5 | | Rt5 | | Imm25 | | | | | | | | | | | DIVUI | | Unsigned divide | |
| 16 | | | Ra5 | | Rt5 | | Imm25 | | | | | | | | | | | DIVSI | | Signed divide | |
| 17 | | | Ra5 | | Rt5 | |  | | | | | | | | Cnd5 | | | TRAPcc | | Trap on condition | |
| 18 | | | Ra5 | | Cond5 | | Imm25 | | | | | | | | | | | TRAPcci | | Trap on condition | |
| 19 | | |  | |  | |  | | | | | | | | | | |  | |  | |
| 20 | Rt5 | | | Imm32 | | | | | | | | | | | | | | SETLO | | Set low order bits | |
| 21 |
| 22 |
| 23 |
| 24 | | Address35 | | | | | | | | | | | | | | | | CALL | | call subroutine | |
| 25 | | Address35 | | | | | | | | | | | | | | | | JMP | | jump | |
| 26 | | Ra5 | | | Rt5 | Address25 | | | | | | | | | | | | JAL | | jump and link | |
| 27 | |  | | |  | Imm22 | | | | | | | | | | 000 | | RET | | return and adjust stack pointer | |
| 28 | Rt5 | | | Imm32 | | | | | | | | | | | | | | SETHI | | Set high order bits | |
| 29 |
| 30 |
| 31 |

|  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Memory Operations | | | | | | | | |
| 32 | Ra5 | | Rt5 | disp25 | | | LB | load byte, sign extend |
| 33 | Ra5 | | Rt5 | disp25 | | | LC | load character, sign extend |
| 34 | Ra5 | | Rt5 | disp25 | | | LH | load half-word, sign extend |
| 35 | Ra5 | | Rt5 | disp25 | | | LW | load word |
| 36 | Ra5 | | Rt5 | disp25 | | | LP | load pair |
| 37 | Ra5 | | Rt5 | disp25 | | | LBU | load byte, zero extend |
| 38 | Ra5 | | Rt5 | disp25 | | | LCU | load character, zero extend |
| 39 | Ra5 | | Rt5 | disp25 | | | LHU | load half-word, zero extend |
| 40 | Ra5 | | Sprt5 | disp25 | | | LSH | load special half-word |
| 41 | Ra5 | | Sprt5 | disp25 | | | LSW | load special word |
| 42 | Ra5 | | Rt5 | disp25 | | | LF | load float |
| 43 | Ra5 | | Rt5 | disp25 | | | LFD | load float double |
| 44 | Ra5 | | Rt5 | disp25 | | | LFP | load float pair |
| 45 | Ra5 | | Rt5 | disp25 | | | LFDP | load float double pair |
| 46 | Ra5 | | Rt5 | disp25 | | | LWR | load word, reserve address |
| 47 |  | |  |  | | |  | reserved |
| 48 | Ra5 | | Rt5 | disp25 | | | SB | store byte (zero) |
| 49 | Ra5 | | Rt5 | disp25 | | | SC | store character |
| 50 | Ra5 | | Rt5 | disp25 | | | SH | store half-word |
| 51 | Ra5 | | Rt5 | disp25 | | | SW | store word |
| 52 | Ra5 | | Rt5 | disp25 | | | SP | store pair |
| 53 | Ra5 | | Rb5 | Rt5 | disp14 | Op6 |  | Indexed memory operations |
| 54 |  | |  |  | | |  | reserved |
| 55 |  | |  |  | | |  | reserved |
| 56 | Ra5 | | Sprs5 | disp25 | | | SSH | store special half-word |
| 57 | Ra5 | | Sprs5 | disp25 | | | SSW | store special word |
| 58 | Ra5 | | Rb5 | disp25 | | | SF | store float |
| 59 | Ra5 | | Rbt5 | disp25 | | | SFD | store float double |
| 60 | Ra5 | | Rb5 | disp25 | | | SFP | store float pair |
| 61 | Ra5 | | Rb5 | disp25 | | | SFDP | store float double pair |
| 62 | Ra5 | | Rb5 | disp25 | | | SWCR | store word, clear address reservation |
| 63 |  | |  |  | | |  |  |
| IO Operations | | | | | | | | |
| 64 | Ra5 | | Rt5 | I/O Address25 | | | INB | input byte, sign extend |
| 65 | Ra5 | | Rt5 | I/O Address25 | | | INCH | input character, sign extend |
| 66 | Ra5 | | Rt5 | I/O Address25 | | | INH | input half-word, sign extend |
| 67 | Ra5 | | Rt5 | I/O Address25 | | | INW | input word |
| 68 | Ra5 | | Rt5 | I/O Address25 | | | INBU | input byte, zero extend |
| 69 | Ra5 | | Rt5 | I/O Address25 | | | INCU | input character, zero extend |
| 70 | Ra5 | | Rt5 | I/O Address25 | | | INHU | input half-word, zero extend |
| 71 |  | |  |  | | |  |  |
| 72 | Ra5 | | Rt5 | I/O Address25 | | | OUTB | output byte |
| 73 | Ra5 | | Rt5 | I/O Address25 | | | OUTC | output character |
| 74 | Ra5 | | Rt5 | I/O Address25 | | | OUTH | output half-word |
| 75 | Ra5 | | Rt5 | I/O Address25 | | | OUTW | output word |
| 76 | Ra5 | | Cmd5 | disp25 | | | CACHE | Cache command |
| 77 | Ra5 | | Rt5 | disp25 | | | LEA | Load effective address |
| 78 | An4 | Reglist31 | | | | | LM | Load multiple registers |
| 79 | An4 | Reglist31 | | | | | SM | Store multiple registers |

|  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Flow Control | | | | | | | | | |
| 80 | Ra5 | Target12 | | | | Imm18 | | BLTI | branch if less than |
| 81 | Ra5 | Target12 | | | | Imm18 | | BGEI | branch if greater or equal |
| 82 | Ra5 | Target12 | | | | Imm18 | | BLEI | branch if less or equal |
| 83 | Ra5 | Target12 | | | | Imm18 | | BGTI | branch if greater than |
| 84 | Ra5 | Target12 | | | | Imm18 | | BLTUI | branch if lower |
| 85 | Ra5 | Target12 | | | | Imm18 | | BGEUI | branch if higher or same |
| 86 | Ra5 | Target12 | | | | Imm18 | | BLEUI | branch if lower or same |
| 87 | Ra5 | Target12 | | | | Imm18 | | BGTUI | branch if higher |
| 88 | Ra5 | Target12 | | | | Imm18 | | BEQI | branch if equal |
| 89 | Ra5 | Target12 | | | | Imm18 | | BNEI | branch if not equal |
| 90 |  |  | | | |  | |  |  |
| 91 |  |  | | | |  | |  |  |
| 92 |  |  | | | |  | |  |  |
| 93 |  |  | | | |  | |  |  |
| 94 | Ra5 | Rb5 | Op5 | Imm20 | | | | Branch to register | |
| 94 | Ra5 | Rb5 | 0 | Imm20 | | | | BLTRI | branch if less than |
| 94 | Ra5 | Rb5 | 1 | Imm20 | | | | BGERI | branch if greater or equal |
| 94 | Ra5 | Rb5 | 2 | Imm20 | | | | BLERI | branch if less or equal |
| 94 | Ra5 | Rb5 | 3 | Imm20 | | | | BGTRI | branch if greater than |
| 94 | Ra5 | Rb5 | 4 | Imm20 | | | | BLTURI | branch if lower |
| 94 | Ra5 | Rb5 | 5 | Imm20 | | | | BGEURI | branch if higher or same |
| 94 | Ra5 | Rb5 | 6 | Imm20 | | | | BLEURI | branch if lower or same |
| 94 | Ra5 | Rb5 | 7 | Imm20 | | | | BGTURI | branch if higher |
| 94 | Ra5 | Rb5 | 8 | Imm20 | | | | BEQRI | branch if equal |
| 94 | Ra5 | Rb5 | 9 | Imm20 | | | | BNERI | branch if not equal |
| 95 |  |  |  |  | | | | Branch to register | |
| 95 | Ra5 | Rb5 | Target20 | | | | 0 | BLT | a < b |
| 95 | Ra5 | Rb5 | Target20 | | | | 1 | BGE | a >= b |
| 95 | Ra5 | Rb5 | Target20 | | | | 2 | BLE | a<=b |
| 95 | Ra5 | Rb5 | Target20 | | | | 3 | BGT | a >b |
| 95 | Ra5 | Rb5 | Target20 | | | | 4 | BLTU | a < b |
| 95 | Ra5 | Rb5 | Target20 | | | | 5 | BGEU | a >=b |
| 95 | Ra5 | Rb5 | Target20 | | | | 6 | BLEU | a <=b |
| 95 | Ra5 | Rb5 | Target20 | | | | 7 | BGTU | a > b |
| 95 | Ra5 | Rb5 | Target20 | | | | 8 | BEQ | a == b |
| 95 | Ra5 | Rb5 | Target20 | | | | 9 | BEQ | a == b |
| 95 | Ra5 | Rb5 | Target20 | | | | 10 | BRA | 1 |
| 95 | Ra5 | Rb5 | Target20 | | | | 11 | BRN | 0 |
| 95 | Ra5 | Rb5 | Target20 | | | | 12 | BAND | a && b |
| 95 | Ra5 | Rb5 | Target20 | | | | 13 | BOR | a || b |
| 95 |  |  | Target20 | | | | 14 | BNR | Reservation flag = 0 |
| 95 |  | Rb5 | Target20 | | | | 15 | LOOP | b <> 0, decrement b |
| 95 | Ra5 | Rb5 | Rc5 | |  | | 16 | BLTR | branch if less than |
| 95 | Ra5 | Rb5 | Rc5 | |  | | 17 | BGER | branch if greater or equal |
| 95 | Ra5 | Rb5 | Rc5 | |  | | 18 | BLER | branch if less or equal |
| 95 | Ra5 | Rb5 | Rc5 | |  | | 19 | BGTR | branch if greater than |
| 95 | Ra5 | Rb5 | Rc5 | |  | | 20 | BLTUR | branch if lower |
| 95 | Ra5 | Rb5 | Rc5 | |  | | 21 | BGEUR | branch if higher or same |
| 95 | Ra5 | Rb5 | Rc5 | |  | | 22 | BLEUR | branch if lower or same |
| 95 | Ra5 | Rb5 | Rc5 | |  | | 23 | BGTUR | branch if higher |
| 95 | Ra5 | Rb5 | Rc5 | |  | | 24 | BEQR | branch if equal |
| 95 | Ra5 | Rb5 | Rc5 | |  | | 25 | BNER | branch if not equal |

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| Relational Compares | | | | | |
| 96 | Ra5 | Rt5 | Imm25 | SLTI | a < b |
| 97 | Ra5 | Rt5 | Imm25 | SGEI | a >= b |
| 98 | Ra5 | Rt5 | Imm25 | SLEI | a <= b |
| 99 | Ra5 | Rt5 | Imm25 | SGTI | a > b |
| 100 | Ra5 | Rt5 | Imm25 | SLTUI | a < b |
| 101 | Ra5 | Rt5 | Imm25 | SGEUI | a >= b |
| 102 | Ra5 | Rt5 | Imm25 | SLEUI | a <= b |
| 103 | Ra5 | Rt5 | Imm25 | SGTUI | a > b |
| 104 | Ra5 | Rt5 | Imm25 | SEQI | a == b |
| 105 | Ra5 | Rt5 | Imm25 | SNEI | a != b |
| 106 |  |  |  |  |  |
| 107 |  |  |  |  |  |

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| 108 | Ra5 | Rb5 | Rt5 |  | Func6 | **FP** |  |
| 108 | Ra5 | Rb5 | Rt5 |  | 0 | FDADD | Addition |
| 108 | Ra5 | Rb5 | Rt5 |  | 1 | FDSUB | subtraction |
| 108 | Ra5 | Rb5 | Rt5 |  | 2 | FDMUL | multiplication |
| 108 | Ra5 | Rb5 | Rt5 |  | 3 | FDDIV | division |
| 108 | Ra5 | Rb5 | Rt5 |  | 4 | FDCUN |  |
| 108 | Ra5 | Rb5 | Rt5 |  | 5 | FDI2F |  |
| 108 | Ra5 | Rb5 | Rt5 |  | 6 | FDF2I |  |
| 108 | Ra5 | Rb5 | Rt5 |  | 7 | FDF2D |  |
| 108 | Ra5 | Rb5 | Rt5 |  | 8 | FDD2F |  |
| 108 | Ra5 | Rb5 | Rt5 |  | 12 | FDCLT | a < b |
| 108 | Ra5 | Rb5 | Rt5 |  | 20 | FDCEQ | a == b |
| 108 | Ra5 | Rb5 | Rt5 |  | 28 | FDCLE | a <= b |
| 108 | Ra5 | Rb5 | Rt5 |  | 36 | FDCGT | a > b |
| 108 | Ra5 | Rb5 | Rt5 |  | 44 | FDCNE | a <> b |
| 108 | Ra5 | Rb5 | Rt5 |  | 52 | FDCGE | a >= b |
|  |  |  |  |  |  |  |  |
| 109 | Ra5 | Rt5 |  |  | Func5 | **FPLOO** | Floating point |
| 109 | Ra5 | Rt5 |  |  | 13 | I2F | Integer to float |
| 109 | Ra5 | Rt5 |  |  | 14 | F2I | Float to integer |
| 110 | Ra5 | Rt5 |  |  | Func5 | **FPZL** | Floating point |
| 110 | Ra5 | Rt5 |  |  | 0 | FABS | Floating point absolute value |
| 110 | Ra5 | Rt5 |  |  | 1 | FNABS | Floating point neg. absolute |
| 110 | Ra5 | Rt5 |  |  | 2 | FNEG | Floating point negate |
| 110 | Ra5 | Rt5 |  |  | 3 | FMOV | Floating point move |
| 110 | Ra5 | Rt5 |  |  | 4 | FSIGN | Floating point get sign |
| 110 | Ra5 | Rt5 |  |  | 5 | FMAN | Floating point get mantissa |
| 110 | Ra5 | Rt5 |  |  | 6 |  |  |
| 110 | Ra5 | Rt5 |  |  | 7 |  |  |
| 110 | Ra5 | Rb5 | Rt5 |  | 8 | FCLT | a < b |
| 110 | Ra5 | Rb5 | Rt5 |  | 9 | FCGE | a >= b |
| 110 | Ra5 | Rb5 | Rt5 |  | 10 | FCLE | a <= b |
| 110 | Ra5 | Rb5 | Rt5 |  | 11 | FCGT | a > b |
| 110 | Ra5 | Rb5 | Rt5 |  | 12 | FCEQ | a == b |
| 110 | Ra5 | Rb5 | Rt5 |  | 13 | FCNE | a <> b |
| 110 | Ra5 | Rb5 | Rt5 |  | 14 | FCUN | Floating point unordered |
| 110 | Ra5 | Rb5 | Rt5 |  | 15 | FCOR | Floating point ordered |

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| 111 | |  |  |  | NOP |  |
| 73 | Imm39 | | | | IMM | Immediate prefix |